A) SISO MAIN CODE

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_unsigned.ALL;

entity SISO is

Port ( in1 : in STD\_LOGIC;

clk : in STD\_LOGIC;

slow\_clk:inout std\_logic;

out1 : out STD\_LOGIC);

end SISO;

architecture Behavioral of SISO is

signal q:std\_logic\_vector(3 downto 0);

signal counter: std\_logic\_vector(25 downto 0):=(others =>'0');

begin

process(slow\_clk,in1)

begin

if(slow\_clk'event and slow\_clk='1')then

q(3 downto 1) <= q(2 downto 0);

q(0)<= in1;

out1 <= q(3);

end if;

end process;

process(clk)

begin

if (clk'event and clk='1')then

counter <=counter+'1';

end if;

end process;

slow\_clk <= counter(0);

end Behavioral;

B) SISO Testbench

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity SISO\_tb is

-- Port ( );

end SISO\_tb;

architecture Behavioral of SISO\_tb is

component SISO is

port( in1 : in STD\_LOGIC;

clk : in STD\_LOGIC;

slow\_clk:inout std\_logic;

out1 : out STD\_LOGIC);

end component;

signal in1,clk,out1,slow\_clk:std\_logic;

begin

U1:SISO port map(in1,clk,slow\_clk,out1);

process

begin

clk <='1';

wait for 50 ns;

clk <='0';

wait for 50 ns;

end process;

process

begin

in1 <='0';

wait for 160 ns;

in1 <='1';

wait for 80 ns;

end process;

end Behavioral;